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FREQUENCY ACQUISITION FOR DATA RECOVERY LOOPS

RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application No. 60/206,191, filed on May 22, 2000. The entire teachings of the above application(s) are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Monolithic data recovery phase locked loops (PLLs) require a large frequency capture range, due to the large frequency deviations of on-chip voltage-controlled oscillators (VCOs) caused by extensive process variations. As the capture range of a loop using only phase correction is limited, a frequency acquisition aid must be used.

One method that has been used is to directly measure the frequency of the VCO output, and when it is close to the target frequency, switch control of the VCO to the data recovery PLL. However, this requires extremely fast circuitry, especially at the high speeds (multi-gigabits per second) required in typical high-speed communication links.

SUMMARY OF THE INVENTION

The design employed by the present invention offers a new frequency acquisition technique which helps the main recovery PLL lock to data stream under considerable process variations.

Accordingly, a frequency monitor includes an edge detector which produces a pulse for each rising or falling edge of an error signal. The error signal itself has a frequency that is responsive to a difference between frequencies of two input signals. A resistive circuit has an effective average resistance that depends on the rate or frequency of the edge detector output pulses. A capacitor holds a charge that depends on the effective average resistance of the resistive circuit. Finally, an indicator circuit produces an output based on the charge held by the capacitor. The indicator circuit output indicates whether the difference between the two input signal frequencies is less than some predetermined amount.

The resistive circuit is implemented in one embodiment as a switched capacitor circuit that charges and discharges at a rate that depends on the rate of the edge detector output pulses.

The indicator circuit is implemented in one embodiment as a comparator that produces the indicator circuit output, which is at one of two levels based on the charge and some threshold, where one level indicating that the difference between the two input signal frequencies is less than a predetermined amount, and the second level indicating that said difference is greater than a predetermined amount.

Furthermore, a selector, responsive to the indicator circuit output, selects from plural sources, for example, a data phase detector circuit and a frequency acquisition circuit, to control an oscillator. The oscillator may be, for example, a voltage-controlled oscillator. It produces a clock signal at a sampling frequency, which is used by the detector circuit to receive data.

The frequency acquisition circuit compares the clock signal with a reference clock to produce a frequency acquisition output indicative of the difference between the frequencies of the reference clock and the oscillator clock signal. The output is one of the sources to the selector.

The data phase detector circuit compares the clock signal with a rate of incoming data to produce a data phase detector output indicative of the difference between the

frequencies of the reference clock and the incoming data. The output another one of the sources to the selector.

In at least one embodiment, the data phase detector circuit output comprises the error signal.

In an alternate embodiment, the error signal is formed by a combiner circuit which combines the two input signals. For example, the combiner circuit can include a mixer which mixes the two input signals to produce a mixed signal, followed by a low-pass filter which filters the mixed signal to produce the error signal.

One advantage of the present invention is that the maximum frequency found in the present invention is equal to the difference between the frequencies of the input signal and the reference clock, which is considerably lower than the signal frequency. Thus, the acquisition loop can operate using standard CMOS technology.

Another advantage is that the frequency acquisition technique of the present invention can be used with any PLL regardless of its architecture. In other words, it is compatible with almost any PLL architecture.

Yet another advantage is that the existence of an input signal and frequency lock condition can be detected.

Finally, the overall architecture requires a very low transistor count and complexity.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

Fig. 1 is a block diagram of a combined phase detector and frequency acquisition loop, with the frequency monitor of an embodiment of the present invention.

Fig. 2 is a simplified schematic diagram for the frequency monitor of Fig. 1.

Fig. 3 is a schematic for the mixer of Fig. 2.

Fig. 4 is a simplified schematic diagram for the edge detector of Fig. 2.

Fig. 5 is a schematic for the hysteresis circuit of Fig. 4.

Fig. 6 is a block diagram of a combined phase detector and frequency acquisition loop, with the frequency monitor of an alternate embodiment of the present invention.

Fig. 7 is a simplified schematic diagram for the frequency monitor of Fig. 6.

DETAILED DESCRIPTION OF THE INVENTION

Fig.1 shows a phase detector circuit 4 together with the frequency acquisition circuit 2.

A voltage-controlled oscillator (VCO) 10 produces a sampling clock 6 at a frequency determined by a control voltage 8. The control voltage is driven by either the phase detector circuit 4 or the frequency acquisition circuit 2, as selected by the frequency monitor 28 through selector 32.

In the data phase detector circuit 4, a data recovery phase detector 12 determines the phase offset of data in an input stream 14 with respect to the sampling clock 6 and produces an error signal V_{er} which is indicative of this phase offset. The output signal 13 drives a first charge pump 18. The output of the charge pump 18, if selected by selector 32, is filtered by loop filter 20, resulting in the VCO control voltage 8.

At chip start-up, the frequency acquisition circuit 2 helps the phase detector circuit 4 acquire lock to a reference clock 34, which is typically available for transmitter clock generation. A standard phase/frequency detector 24 compares the reference clock 34 with the VCO output 6, or a sub-harmonic thereof, and produces a voltage 25 indicative of the frequency difference between the two signals. This voltage 25 then drives a second charge pump 26 whose output, if selected by selector 32, is filtered by loop filter 20, resulting in the VCO control voltage 8.

The frequency acquisition circuit 2 thus acts to rapidly force the VCO to operate close to the reference clock 34 frequency. During this time, selector 32 connects the

second charge pump 26 to the loop filter 20 so that the frequency acquisition circuit 2 is driving the VCO 10.

The frequency monitor 28 continuously compares the frequency $f_{\phi ref}$ of the reference clock ϕ_{ref}, which is close to the incoming data frequency, to the frequency $f_{\phi vco}$ of the VCO output ϕ_{vco} 6, and keeps the frequency acquisition circuit 2 active as long as the difference between the two frequencies, i.e., $f_{er} = f_{\phi ref} - f_{\phi vco}$, is greater than the frequency capture range of the data recovery circuit 14. When the frequency difference f_{er} is less than the data recovery circuit capture range, the frequency monitor 28 asserts an indicator signal V_Q 30 which causes selector 32 to switch the loop control from the frequency acquisition circuit 2 to the data recovery circuit 4.

Fig. 2 presents a simplified schematic of the frequency monitor 28 of Fig. 1. A mixer 40 combines the reference clock ϕ_{ref} (with frequency $f_{\phi ref}$) and the VCO output ϕ_{vco} (having frequency $f_{\phi vco}$) frequencies to produce a signal V_{out} that contains two frequency components: $f_{\phi ref} - f_{\phi vco}$ and $f_{\phi ref} + f_{\phi vco}$. A low-pass filter 42 following the mixer suppresses the component at $f_{\phi ref} + f_{\phi vco}$ and passes the component at $f_{\phi vco}$ in its output V_{er}.

Edge detector 50 generates a full-swing pulse at 51 corresponding to each edge of V_{er} at its input. Thus, the output of the edge detector 50 is a train of pulses at twice the input frequency f_{er}.

The output of the edge detector, shown as dotted line 51, is applied to a switched-capacitor circuit as shown in the dashed box 52 of Fig.2, comprising capacitor C_1 and two complementary switches 53A and 53B, in which one switch turns off when the other switch is on. The effective conductance of the switched-capacitor structure is proportional to the value of capacitance C_1 and the input frequency:

$$G_{switchedcap} = C_1 \cdot f_{er} \qquad \text{(Eq. 1)}$$

and the effective resistance of the structure is:

$$R_{switchedcap} = \frac{1}{C_1 \cdot f_{er}} \qquad \text{(Eq. 2)}$$

Capacitor C_2 is placed at the output of the switched-capacitor structure to reduce the switching noise to the input V_{sw} of comparator 58. The fixed current source 56 supplies a constant current I into the switched-capacitor circuit 52. Thus, the voltage V_{sw} is equal to:

$$V_{sw} = R_{switchedcap} \cdot I \qquad \text{(Eq. 3)}$$

If there is a sufficient difference between the frequencies of the VCO clock 6 and the frequency $f_{\phi ref}$ of the reference clock ϕ_{ref}, i.e., if f_{er} is sufficiently large, the edge detector 50 generates pulses at a high-frequency rate that result in high conductance/low resistance (Equations 1 and 2) of the switched-capacitor structure. The current source I 56 is adjusted such that for f_{er} larger than a certain threshold, i.e., larger than the frequency capture range of the main data recovery loop, the switched-capacitor circuit 52 maintains the voltage V_{sw} below the threshold of comparator 58. Thus, the comparator output V_Q is held at 0. Referring back to Fig. 1, this value of V_Q will direct selector 32 to allow the frequency acquisition circuit 4 to control the VCO 10.

When f_{er} drops below a certain threshold, indicating that the VCO output frequency is within the data recovery capture range, the pulse rate of the edge detector 50 decreases such that the resistance of the switched-capacitor circuit 52 increases. The voltage V_{sw} thus rises above the threshold of the comparator 58. The comparator output V_Q becomes 1, and the selector 32 hands loop control to the data phase detector circuit 2.

The frequency acquisition circuit 4 will become active again, i.e., reselected, if the VCO frequency drifts away from the target frequency (that is, $f_{\phi ref}$, which is the same or very close to the expected data frequency) by more than a certain amount.

One major benefit of this embodiment is that it can be used with any type of data recovery loop circuit, independent of its architecture and data phase detector.

Fig. 3 is a circuit schematic for the mixer 40 of Fig. 2. A differential VCO output 6A, 6B is applied to transistors 60 - 63. A differential reference clock signal 34A, 34B is applied to the respectively to the gates of transistors 60 and 63, and 61 and

62. Note that the gate controls of transistors 61 and 63 are inverted. The effect is that ϕ_{vco} is modulated by ϕ_{ref}, such that the differential output V_{out} contains frequency components which are the sum and difference of the corresponding frequencies $f_{\phi vco}$ and $f_{\phi ref}$.

Fig. 4 is a block diagram of the edge detector 50 of Fig. 2. As Fig. 4 illustrates, the edge detector 50 is designed to have a hysteresis characteristic 70, using positive feedback in its first stage amplifier 78. Thus, it reacts only to oscillation amplitudes larger than a certain threshold level. This helps to prevent erroneous transitions due to noise.

For example, at 80 is shown a signal oscillating with an amplitude larger than the necessary threshold level. The hysteresis circuit 70 magnifies the oscillations as shown at 82. A level converter 72 converts the oscillations to square pulses 84, while the combination of delay 74 and XOR gate 76 create a pulse for each transition of the output 85 of the level converter 72, as shown at 86.

On the other hand, at 90 is shown a noise signal with an amplitude which is less than the threshold level. Resulting waveforms shown at 92, 94 and 96 respectively, illustrate that the circuit does not respond to this noise 90.

Fig. 5 is a circuit schematic of the hysteresis circuit 70 of Fig. 4. Current source 104 draws current through the circuit. A differential front-end amplifier, comprising devices 102, modulates based on the input signal, which corresponds to the output V_{out} of the mixer 28 of Fig. 3. A diode-connected PMOS device 101 in series with each input amplifier 102 acts as an active resistor. In parallel with each diode-connected device 101 is a second PMOS device 103 which is biased by a cross-coupling to the other side of the differential circuit, to provide positive feedback. To ensure hysteresis behavior in the front-end amplifier, i.e., devices 102, the size W_2 of the cross-coupled PMOS devices 103 should be larger than the size W_1 of the diode-connected PMOS devices 101.

The present invention can be used with any PLL regardless of its architecture. It can thus be used to recover the frequency information of random-pattern data, which is

not possible using conventional phase-frequency detectors. In addition, this design is suitable for very high-speed application, as it operates at a much lower speed than the high-speed input signal, and can be implemented using standard CMOS technology. Another benefit is that the overall architecture requires a very low transistor count and complexity.

A second embodiment is illustrated in Figs. 6 and 7. In this embodiment, the frequency monitor 28 uses cycle-slipping information from an analog data phase detector 112 to indicate when the VCO's output frequency is different from that of the incoming data. Such an analog data phase detector is described in a U.S. Patent Application, filed on the even day herewith, entitled "A LINEAR DATA PHASE RECOVER DETECTOR" to Ramin Farjad-Raj, attorney's docket number 2789.2017-000.

During cycle-slipping, sweeping of the VCO clock phases over the data stream causes the phase detector output V_{er} 16 to oscillate between "early" and "late" signals. The frequency of this oscillation (sweep speed) is equal to the frequency difference between the receive clock and the incoming data.

This V_{er} can be used directly by a frequency monitor 128 which is appropriately modified from that of Figs. 1 and 2. Thus, in this embodiment, the frequency monitor 128 does not need direct access to the VCO output 6 and the reference clock 34.

Fig. 7 is a block diagram of the modified frequency monitor 128. It is essentially the same as that of Fig. 2, with the exception that the mixer and low-pass filter are no longer needed.

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.